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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,729	10/29/2003	Hoang T. Tran	1875.4520000	4015

26111 7590 08/06/2008

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
SUN, SCOTT C	
ART UNIT	PAPER NUMBER
2182	
MAIL DATE	DELIVERY MODE
08/06/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/694,729	TRAN ET AL.	
	Examiner	Art Unit	
	SCOTT SUN	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/5/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendments to the claims filed 5/5/2008 has been noted and entered.

Response to Arguments

2. Applicant's arguments filed 5/5/2008 have been fully considered but they are not persuasive. Applicant's arguments are summarized as:

a. Prior art of record does not disclose parallel input or serial output, but only serial input and parallel output.

b. Prior art of record does not disclose the pad functioning as both input or output based on said protocol and electrical specification instructions.

c. Prior art of record does not disclose that input and output still function after the protocol and electrical configurations.

3. In response to argument 'a', examiner notes that Weber discloses the system being able to support multiple protocols and more specifically STMS (single-thread, multi-speed) which is a serial protocol, and MTSS (multi-thread, single speed) which is a parallel protocol (paragraph 2-3). Although internally, the serial data received is converted to parallel for processing, the multi-protocol system of Weber receives both parallel and serial data, and outputs the same. This is done by using multiple threads to perform the MTSS protocol input process (paragraph 18). Similarly, on transmission, only one thread is used for the serial transmission of STMS protocol (paragraph 25).

Therefore, the system of Weber contains both serial and parallel ports, and both of capable of inputting and outputting data.

4. In response to argument 'b', examiner notes that the claim clearly states input and output in the alternative using "or". There is no requirement that the pad supports both input and output functions. Even assuming such a limitation, examiner notes that as stated for argument 'a', the system including a plurality of threads that perform the input and output functions, as well as parallel and serial protocols.

5. In response to argument 'c', examiner notes that Weber's system functions for two distinct protocols, and dynamically adjusts between the two types of protocols. Although not explicitly stated, but it is clearly implied that after adjusting from one protocol to another, the system still functions. And therefore, the system still sends and receives data after the configurations are done.

6. Having responded to each of applicant's arguments, examiner notes that prior art of record still provide a valid ground of rejection, attached below with modifications made in response to the claim amendments. New rejections are added for the newly added claims 31-38.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 12, 15, 16, 18-20, 25-27, and 31-38 are rejected under 35 U.S.C. 102(e) as being unpatentable Weber et al (hereinafter, Weber, PG Pub #2003/0120791) in view of Cliff et al (hereinafter, Cliff, PG Pub #2001/0017595).

9. Regarding claim 12, Weber discloses a transceiver (system 400 in figure 4), comprising:

a plurality of ports, wherein said plurality of ports includes at least one parallel port and at least one serial port (serializer/deserializers 410-413 functioning in serial or parallel for STMS or MTSS protocol, figure 4, paragraph 18 and 25);

a bus (connections between the various elements in figure 4) connecting said plurality of ports on a common substrate (single die, line 8, paragraph 22) wherein said bus is configured to connect the at least one parallel port to at least one second parallel port or to said at least one serial port (all SERDES are interconnected as shown in figure 4);

a plurality of programmable pads (data presenters 460-463, and aggregators 440-443 and corresponding encoder 470-473/decoders 420-423, figure 4) in communications with said plurality of ports (lines 1-9, paragraph 23);

a register (register bits, line 17, paragraph 24) for sending instructions to configure at least one of said programmable pads to comply with a specified data protocol (STMS, Fibre, Ethernet, etc) and the specified electrical specification (serial/parallel, different bit rates of each protocol). Examiner notes that Weber discloses the data presenters and aggregators are instructed to process data according

to the desired protocol definition and its transfer rate (data aggregators configured to receive data, lines 1-9, paragraph 23; data presenters configured to send data, lines 1-9, paragraph 25).

Wherein at least one of said programmable pads is configured to either send or receive data after having been configured to comply with said data protocol and electrical specification ("aggregator 440-443 receive data stored in buffers and align the data properly according to a desired protocol definition", lines 7-9, paragraph 23).

Weber does not disclose explicitly the electrical specifications include configuring an operating voltage. However, Cliff discloses configuring an operating voltage for a programmable logic device (programmable voltage regulator 310, figure 3; paragraph 29, 32). Teachings of Weber and Cliff are from the same field of programmable circuits.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Weber and Cliff by adding programmable voltage regulator into the system of Weber for the benefit of efficiently retrofitting the programmable device (paragraph 29, Cliff).

10. Regarding claim 15, Weber and Cliff combined disclose claim 12 and Weber further discloses an input controller (protocol processors 450-455) for configuring at least one of said programmable pads to receive at least one of a data signal and a control signal (lines 6-11, paragraph 16, lines 1-9, paragraph 23).

11. Regarding claim 16, Weber and Cliff combined disclose claim 12 and Weber further discloses an output controller (protocol processors 450-455) for configuring at

least one of said programmable pads to send at least one of a data signal and a control signal (lines 1-6, paragraph 17, 1-11, paragraph 24).

12. Regarding claims 18-20 and 25-27, examiner notes that these claims contain limitations substantially similar to those in claims 12, 15 and 16. The same grounds of rejection are applied.

13. Regarding claims 31, 33, and 36, examiner notes that Weber discloses using 10 Gb Ethernet as an exemplary embodiment. Other 10 Gb protocols would be obvious design choices given the teachings of Weber (paragraph 28).

14. Regarding claim 32, Weber and Cliff combined disclose claim 1, and Weber further discloses wherein said at least one parallel port is configured to operate at 1/10 of a data rate of said at least one serial port (paragraph 23). Examiner notes that Weber discloses serial data are converted to lower speed parallel data, and one of ordinary skill would readily recognize that 10 bit coding parallel data are 1/10 of the speed of its serial counterpart.

15. Regarding claim 34, Weber and Cliff combined disclose claim 1, and Weber further discloses at least one serial port is configured to operate at a plurality of data rates (paragraph 14).

16. Regarding claim 35, Weber and Cliff combined disclose claim 34, and examiner notes that the data rates are obvious design choices given the teachings of Weber to have variable rates of data transfer (paragraph 26).

17. Regarding claim 37 and 38, Weber and Cliff combined disclose claim 1, and Weber further discloses serial/parallel conversion (serializers and deserializers in figure 4).

18. Claims 17, 21, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weber in view of Cliff and further in view of Rearick et al (hereinafter Rearick, PG Pub #2003/0172332).

19. Regarding claim 17, Weber and Cliff combined disclose claim 12 but do not disclose explicitly measuring leakage current. However, Rearick discloses a testing register (driver test system 200, figure 2) for sending a test message to measure leakage current (tri-state leakage current) from at least one of a programmable pad (paragraphs 33, 40). Teachings of Weber, Cliff and Rearick are from the same field of integrated circuits.

Therefore, it would have been obvious at the time of invention to combine teachings of Weber, Cliff and Rearick by adding Rearick's testing circuit to the combined system of Weber and Cliff for the benefit of providing cost-effective and accurate self-testing capability to the integrated circuit (background, Rearick).

20. Regarding claims 21 and 28, examiner notes that these claims contain limitations substantially similar to those in claim 17. The same grounds of rejection are applied.

21. Claims 13, 14, 22-24, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weber in view of Cliff and further in view of Taniguchi et al (hereinafter Taniguchi, PG Pub #2001/0015664).

22. Regarding claim 13, Weber and Cliff combined disclose claim 12 but do not disclose explicitly adjusting a delay between input and output. However, Taniguchi discloses a timing controller (delay adjustment circuit, figure 5) for modulating delay between input (input buffer) and output (output buffer) of an integrated circuit (DLL Array 7; paragraphs 52, 53). Teachings of Weber, Cliff and Taniguchi are from the same field of integrated circuits.

Therefore, it would have been obvious at the time of invention to combine teachings of Weber, Cliff and Taniguchi by using the adjustable delay circuit disclosed by Taniguchi in the combined system of Weber and Cliff for the benefit of underflow and overflow prevention (paragraph 87, Taniguchi).

23. Regarding claim 14, Weber and Cliff combined disclose claim 12, and Taniguchi further discloses a timing register for sending instructions to adjust the delay between input and output of at least one of said programmable pads. Examiner notes that the same reasons to combine the teachings of Weber and Taniguchi can be applied.

24. Regarding claims 22-24 and 29-30, examiner notes that these claims contain limitations substantially similar to those in claim 13 and 14 above. The same grounds of rejection are applied. Further regarding claims 23 and 24, Examiner notes that Taniguchi discloses that the data is delayed in a buffer (input/output buffer), where the delay is a fixed time interval set by the delay adjustor circuit (figure 5, paragraphs 9, 52).

Conclusion

25. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SCOTT SUN whose telephone number is (571)272-2675. The examiner can normally be reached on Mon-Thu, 10:00am-8pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tariq Hafiz can be reached on (571) 272-6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

/Tariq Hafiz/
Supervisory Patent Examiner, Art Unit 2182